CLAIM AMENDMENTS

1. (Original) Computer-readable media containing a program which, when read and executed by a computer, causes the computer to synthesize a clock tree for a partitioned integrated circuit (IC) layout comprising a plurality of base level partitions and a top level partition each occupying a separate area of a semiconductor substrate, wherein the base level partitions comprise syncs to be clocked by edges of a clock signal applied to an entry node within the area occupied by the top level partition, the computer-readable media comprising:

first computer instructions for causing the computer to separately synthesize a plurality of independently balanced subtrees, each subtree corresponding to a separate base level partition and comprising a start point at a perimeter of the area occupied by that base level partition and a network of buffers and signal paths for conveying a clock signal edge from the start point to each sync included within that area; and

second computer instructions for causing the computer to synthesize a top level portion of the clock tree for conveying the clock signal from the entry point to the start point of each synthesized subtree.

2. (Original) The computer readable media in accordance with claim 1

wherein each subtree has an average clock signal path delay that is an average of clock signal path delays between the subtree's start point and all syncs within the corresponding base level partition,

wherein at least two of the subtrees have substantially dissimilar average clock signal path delays, and

wherein path delays of paths within the top level portion of the clock tree linking the entry node to the start point of each subtree compensate for differences in average path delays of the subtrees so as to substantially equalize clock signal path delays between the entry point and all syncs.

3. (Original) The computer-readable media in accordance with claim 1 wherein the top level partition also includes syncs, the computer-readable media further comprising:

instructions for causing the computer to synthesize a balanced subtree of the clock tree for the top level partition for delivering the clock signal from a start point within the area of the substrate occupied by the top level partition to each sync included within the top level partition,

wherein the synthesized top level portion of the clock tree also conveys the clock signal from the entry point to the start point of the synthesized subtree for the top level partition.

4. (Previously Presented) The computer-readable media in accordance with claim 1 wherein the subtrees have substantially differing average clock signal path delays, each subtree's average clock signal path delay being defined as an average of clock signal path delays between that subtree's starting point and all syncs within the corresponding base level partition, and wherein the second computer instructions comprises:

computer instructions for causing the computer to select a first base level partition and a second base level partition from among the plurality of base level partitions,

computer instructions for causing the computer to synthesize a first signal path linking the start point of the subtree of first base level partition to a first node within the top level partition, and

computer instructions for causing the computer to synthesize a second signal path linking the start point of the subtree of the second base level partition to the first node,

wherein the first and second signal paths provide substantially differing path delays between the
first node and the start points of the subtrees of the first and second partitions to compensate for the substantially differing average clock signal path delay of the subtrees of the first and second base level partitions so that a clock signal edge departing the first node will arrive at each sync within the first and second base level partitions at substantially the same time.

5. (Original) The computer-readable media in accordance with claim 4 wherein the second instructions cause the computer to adjust path delays of the first and second signal paths to compensate for the substantially differing clock signal path delays of the subtrees of

the first and second partitions by adjusting at least one of the following:

a number of buffers included in the paths,

a size of at least one buffer included in the path,

a position of at least one buffer included in the path, and

a position of the selected node relative to the start points of the first and second trees.

6. (Currently Amended) The computer-readable media in accordance with claim 4 wherein the second instructions cause the computer to adjust path delays of the first and second signal paths to compensate for the substantially differing clock signal path delays of the subtrees of the first and second base level partitions by adjusting all of the following:

a number of buffers included in the paths,

a size of at least one buffer included in the ~~path~~ paths,

a position of at least one buffer included in the ~~path~~ paths, and

a position of the selected node relative to the start points of the subtrees of the first and second ~~trees~~ base level partitions.

7. (Original) The computer-readable media in accordance with claim 6 wherein the second instructions further comprise:

computer instructions for causing the computer to select a third base level partition from among the plurality of base level partitions,

computer instructions for causing the computer to synthesize a third signal path linking the first node to a second node within the top level partition, and

computer instructions for causing the computer to synthesize a fourth signal path linking the subtree of the third base level partition to the second node,

wherein the third and fourth signal paths provide substantially differing path delays to compensate for substantially differing average clock signal path delays of the subtrees of the first, second and third partitions so that a clock signal edge departing the second node will arrive at each sync within the first, second and third partitions at substantially the same time.

8. (Previously Presented) The computer-readable media in accordance with claim 7 wherein th second instructions cause the computer to adjust path delays of the third and fourth signal paths to compensate for the substantially differing clock signal path delays of the subtrees of the first and second partitions by adjusting at least one of the following:

a number of buffers included in the paths,

a size of at least one buffer included in the path,

a position of at least one buffer included in the path, and

a position of the selected node relative to the start points of the first and second trees.

9. (Original) A method for synthesizing a clock tree for a partitioned integrated circuit (IC) layout comprising a plurality of base level partitions and a top level partition each occupying a separate area of a semiconductor substrate, wherein the base level partitions comprise syncs to be clocked by edges of a clock signal applied to an entry node within the area occupied by the top level partition, the method comprising the steps of:

a. separately synthesizing a plurality of independently balanced subtrees, each subtree corresponding to a separate base level partition and comprising a start point at a perimeter of the area occupied by that base level partition and a network of buffers and signal paths for conveying a clock signal edge from the start point to each sync included within that area; and

b. synthesizing a top level portion of the clock tree for conveying the clock signal from the entry point to the start point of each synthesized subtree.

10. (Original) The method in accordance with claim 9

wherein each subtree has an average clock signal path delay that is an average of clock signal path delays between the subtree's start point and all syncs within the corresponding base level partition,

wherein at least two of the subtrees have substantially dissimilar average clock signal path delays, and

wherein path delays of paths within the top level portion of the clock tree linking the entry node to the start point of each subtree compensate for differences in average path delays of the subtrees so

as to substantially equalize clock signal path delays between the entry point and all syncs.

11. (Original) The method in accordance with claim 9 wherein the top level partition also includes syncs, the method further comprising the step of:

c. synthesizing a balanced subtree of the clock tree for the top level partition for delivering the clock signal from a start point within the area of the substrate occupied by the top level partition to each sync included within the top level partition,

wherein the synthesized top level portion of the clock tree also conveys the clock signal from the entry point to the start point of the synthesized subtree for the top level partition.

12. (Previously Presented) The method in accordance with claim 9 wherein the synthesized subtrees have substantially differing average clock signal path delays, each subtree's average clock signal path delay being defined as an average of clock signal path delays between that subtree's starting point and all syncs within the corresponding base level partition, and wherein step b comprises the substeps of:

b1. selecting a first base level partition and a second base level partition from among the plurality of base level partitions,

b2. synthesizing a first signal path linking the start point of the subtree of first base level partition to a first node within the top level partition, and

b3. synthesizing a second signal path linking the start point of the subtree of the second base level partition to the first node,

wherein the first and second signal paths provide substantially differing path delays between the first node and the start points of the subtrees of the first and second partitions to compensate for the substantially differing average clock signal path delay of the subtrees of the first and second base level partitions so that a clock signal edge departing the first node will arrive at each sync within the first and second base level partitions at substantially the same time.

13. (Original) The method in accordance with claim 12 wherein the path delays of the first and second signal paths are adjusted at steps

b2 and b3 to compensate for the substantially differing clock signal path delays of the subtrees of the first and second partitions by adjusting at least one of the following:

a number of buffers included in the paths,

a size of at least one buffer included in the path,

a position of at least one buffer included in the path, and

a position of the selected node relative to the start points of the first and second trees.

14. (Currently Amended) The method in accordance with claim 12 wherein the path delays of the first and second signal paths are adjusted at steps b2 and b3 to compensate for the substantially differing clock signal path delays of the subtrees of the first and second base level partitions by adjusting all of the following:

a number of buffers included in the paths,

a size of at least one buffer included in the ~~path~~ paths,

a position of at least one buffer included in the ~~path~~ paths, and

a position of the selected node relative to the start points of the subtrees of the first and second ~~trees~~ base level partitions.

15. (Original) The method in accordance with claim 12 wherein step b further comprises the substeps of:

b4. selecting a third base level partition from among the plurality of base level partitions,

b5. synthesizing a third signal path linking the first node to a second node within the top level partition, and

b6. synthesizing a fourth signal path linking the subtree of the third base level partition to the second node,

wherein the third and fourth signal paths provide substantially differing path delays to compensate for substantially differing average clock signal path delays of the subtrees of the first, second and third partitions so that a clock signal edge departing the second node will arrive at each sync within the first, second and third partitions at substantially the same time.

16. (Original) A method for generating a layout of an integrated circuit (IC) within a semiconductor substrate, wherein the IC specifies a plurality of base level partitions that are to occupy

non-overlapping areas of the substrate and a top level partition that is to occupy all portions of the substrate external to the areas occupied by the base level partitions, wherein the base level partitions include syncs to be clocked by edges of a clock signal to be applied to a clock signal entry node of the top level partition, and wherein the IC is to include a clock tree comprising buffers and signal paths formed in the substrate for delivering each edge of the clock signal from the entry node to all syncs at substantially the same time, the method comprising the steps of:

a. separately generating a layout for each base level partition and for the top level partition;

b. separately synthesizing a balanced subtree of the clock tree for each base level partition, wherein the balanced subtree for each base level partition comprises a network of buffers and signal paths for delivering the clock signal from a start point at a perimeter of the area of the substrate occupied by the base level partition to each sync included within the base level partition;

c. separately adjusting the layout of each base level partition to place and route therein the buffers and signal paths forming the subtree synthesized for that base level partition at step b; and

d. synthesizing a top level portion of the clock tree residing within the area of the substrate occupied by the top level partition, the top level portion of the clock tree being designed to convey the clock signal from the entry point to the start points of all synthesized subtrees.

17. (Original) The method in accordance with claim 16 further comprising the step of:

e. adjusting the layout of the top level partition to place and route buffers and signal paths forming the top level portion of the clock tree.

18. (Original) The method in accordance with claim 17 further comprising the step of:

f. combining the layouts for the base level partitions and the top level partition to form a layout for the entire IC.

19. (Original) The method in accordance with claim 16 further comprising the step of:

e. synthesizing a balanced subtree of the clock tree for the top level partition for delivering the clock signal from a start point within the area of the substrate occupied by the top level partition to each sync included within the top level partition,

wherein the top level portion of the clock tree synthesized at step d also conveys the clock signal from the entry point to the start point of the subtree synthesized for the top level partition.

20. (Original) The method in accordance with claim 16 wherein step d comprises the substeps of:

d1. selecting a first base level partition and a second base level partition from among the plurality of base level partitions;

d2. synthesizing a first signal path linking a start point of a first subtree synthesized at step c for the first base level partition to a first node within the top level partition; and

d3. synthesizing a second signal path linking a start point of a second subtree synthesized at step c for the second base level partition to the first node,

wherein the first and second signal paths provide substantially differing path delays to compensate for substantial differences in average clock signal path delay of the first and second subtrees so that a clock signal edge departing the first node will arrive at each sync connected to the first and second subtrees at substantially the same time, wherein each subtree's average clock signal path delay is an average of clock signal path delays between that subtree's starting point and all syncs to which that subtree delivers the clock signal.

21. (Original) The method in accordance with claim 20 wherein the path delays of the first and second signal paths are adjusted by adjusting at least one of the following:

a number of buffers included in each of said first and second signal paths,

a size of at least one buffer included in each of said first and second signal paths,

a position of at least one buffer included in each of said first and second signal paths, and

a position of the first node relative to the start points of the first and second trees.

22. (Original) The method in accordance with claim 20 wherein the path delays of the first and second signal paths are adjusted by adjusting all of the following:

a number of buffers included in each of said first and second signal paths,

a size of at least one buffer included in each of said first and second signal paths,

a position of at least one buffer included in each of said first and second signal paths, and

a position of the first node relative to the start points of the first and second trees.

23. (Original) The method in accordance with claim 20 wherein step d further comprises the substeps of:

d4. selecting a third base level partition from among the plurality of base level partitions,

d5. synthesizing a third signal path linking the first node to a second node within the top level partition,

d6. synthesizing a fourth signal path linking a third subtree synthesized at step c for the third base level partition to the second node,

wherein the third and fourth signal paths provide substantially differing path delays to compensate for substantial differences in average clock signal path delay of the third and fourth subtrees so that a clock signal edge departing the second node will arrive at each sync connected to the first, second and third subtrees at substantially the same time.

24. (Original) The method in accordance with claim 16

wherein the subtree for each base level partition delivers each clock signal edge arriving at the subtree's start point to all syncs within the base level partition at substantially the same time,

wherein the subtrees synthesized for the base level partitions have substantially differing average clock signal path delays, wherein each subtree's average clock signal path delay is defined as an

average of clock signal path delays between the subtree's starting point and all syncs to which the subtree delivers the clock signal, and

wherein the synthesized top level portion of the clock tree includes path delays compensating for differences in average path delays of the subtrees so as to substantially equalize clock signal path delays between the entry point and all syncs.